EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"5559967".pn.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:04
S2	570	((ieee adj "1394") adj "1995")	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:05
S3	84	(1394a adj "2000") (1394b adj "2002")	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:05
S4	25	S2 and S3	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 12:03
S5	20	S2 same S3	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:05
S6	16	S2 with S3	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:47
S7	5	("5264958" "20050036506" "20050021890" "20030067884" "6037828").pn.	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:53
S8	3	S7 and ieee	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 10:53
S9	4	S2 and S3 and transceiver	US-PGPUB; USPAT; EPO; JPO	OR	OFF	2006/03/17 12:03

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L1: Entry 11 of 11 File: USPT Nov 23, 1993

DOCUMENT-IDENTIFIER: US 5264958 A
TITLE: Universal communications interface adaptable for a plurality of interface standards

Brief Summary Text (9):
In other DTEs and DCEs, this problem is solved by having a separate cable for each of the interface standards and by routing the signals, depending upon which standard is being used, to a corresponding receiver or set of receivers. For example, a common connector is used at the interchange interface. A group of pins on that connector is dedicated to signals which are unique to the EIA-232-D interface standard. Those signals are routed to a particular receiver or set of receivers configured to receive those signals and convert them to transistor-transistor logic (TTL) level so that a communications processor in the DTE or DCE may process them. Another group of pins are dedicated to those signals unique to the RS-422-A electrical interface standard. Similarly, those RS-422-A signals are routed to receiver(s) configured to convert those signals to TTL level. The same is true for the V.35 standard and so forth. A switch is utilized to switch the appropriate receiver outputs to the communications processor. Cable identification (ID) bits in the cable are used by the switch to identify which electrical interface is being used. This method, however, consumes too much board and connector space and requires unneeded components.

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L1: Entry 1 of 11 File: PGPB Feb 17, 2005

DOCUMENT-IDENTIFIER: US 20050036506 A9
TITLE: Apparatus & method for automatically switching media connections when operating in forced speed and duplex mode

PRIOR-PUBLICATION:

DOC-ID	DATE
US 0174726 A1	September 18, 2003

Summary of Invention Paragraph:
[0003] Most LAN standards address this by assigning different connector pins to the wires in the twisted pair cable which is typically referred to as the Media Dependent Interface (MDI). In the IEEE-802.3's 10BASE-T standard, an end node will assign pins 1 and 2 to the transmit pair, while pins 3 and 6 are for connection to a twisted pair for receiving. The repeater for a 10BASE-T network will assign its transmitter to pins 3 and 6, while its receiver will be connected to pins 1 and 2. This works very well for general configurations where NICs are attached to repeaters. However, there are a few cases that become more important to consider as the emergence of switched networks takes place. First, there is a case where the NIC is connected directly to another NIC, or a repeater is connected to repeater, or a repeater is connected to a switch. Depending on the assignment of pins at the product's network interface, it may become necessary to employ a "crossover" cable to address the fact that both products employ the same pin designations on their interfaces.

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L1: Entry 2 of 11 File: PGPB Jan 27, 2005

DOCUMENT-IDENTIFIER: US 20050021890 A1
TITLE: Multi-functional port

Summary of Invention Paragraph:
[0008] In other DTEs and DCEs, this problem is solved by having a separate cable for each of the interface standards and by routing the signals, depending upon which standard is being used, to a corresponding receiver or set of receivers. In this example, a common connector is used at the interchange interface and has a group of pins dedicated to signals that are unique to each interface standard. This method, however, requires larger connector space.

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L1: Entry 5 of 11 File: PGPB Apr 10, 2003

DOCUMENT-IDENTIFIER: US 20030067884 A1
TITLE: Dynamic detection of LAN network protocol

Detail Description Paragraph:
[0063] Referring to FIG. 7, a more cost effective solution is the second and preferred embodiment of the present invention, which provides a multi-protocol NIC 200e with a configurable, pico-processor or state machine based entities 283, 285. The NIC 200e contains the same bus connector 210 block, bus master interface 212 block, FIFO storage 234 block, and magnetics and connector 270 block as NIC 200a, 200b, and 200c. However, pico-processor controlled buffer management 283 is a new configurable entity that is capable of doing the same functions provided by all three buffer management entities 243, 253, and 263 of NIC 200d (FIG. 6). Likewise, pico-processor controlled status & control section 285 is a new configurable entity that is capable of doing the same functions provided by all three status & control sections 245, 255, and 265 of NIC 200d. The buffer management 283 and status & control 285 are programmable entities that are controlled by a pico-processor, such that blocks 283 and 285 are adaptable to any network specific functions required to support Ethernet, Token-Ring, or ATM networks. NIC 200e has independent entities 246, 256, 266 for each of the MAC protocols, since they each have very specific requirements. A common physical transceiver 288 is used, as this is considered viable in the state-of-the-art technology. The approach works equally well with independent transceiver entities 248, 258, and 268 of FIG. 6 replacing transceiver 288. The protocol selection logic 224 performs the four step process detailed in FIG. 4. However, the protocol selection logic of NIC 200e is slightly different than the protocol selection logic 220 of NIC 200d (FIG. 6) in that it does not perform any operations in parallel. Due to the use of common functions for pico-processor controlled entities 283, 285, the process must be followed in a sequential manner as shown in FIG. 4.

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L1: Entry 10 of 11 File: USPT Mar 14, 2000

DOCUMENT-IDENTIFIER: US 6037828 A
TITLE: Transmission line driver with high output impedance at power off

Brief Summary Text (6):
In order to provide a circuit that complies with different transmission line protocols, some circuits combine the various drivers on the same chip. For a transmitter-receiver circuit, for example, it is desirable to be able to share resources to achieve programmability, or to otherwise reduce cost (reduce package pin count, etc.). However, the power off current associated with the V.35 driver circuit shown in FIG. 1 would make this circuit unacceptable when the same output terminals are to be shared by, for example, an RS232 (V.28) driver. Therefore, this circuit would not allow the transmitter-receiver chip to programmably connect the appropriate driver the same pair of output pins that connect to the transmission line.